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SiO_2/SiC interface proved by positron annihilation

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Abstract

We have studied positron annihilation in a Silicon carbide (SiC)–metal/oxide/semiconductor (MOS) structure using a monoenergetic positron beam. The Doppler broadening of annihilation quanta were measured as functions of the incident positron energy and the gate bias. Applying negative gate bias, significant increases in *S*-parameters were observed. This indicates the migration of implanted positrons towards SiO_2/SiC interface and annihilation at open-volume type defects. The behavior of *S*-parameters depending on the bias voltage was well correlated with the capacitance–voltage (*C*–*V*) characteristics. We observed higher *S*-parameters and the interfacial trap density in MOS structures fabricated using the dry oxidation method as compared to those by pyrogenic oxidation method.

Keywords: SiO_2/SiC interface; MOS structure; Positron beam; Doppler-shift; Open-volume defect

1. Introduction

Silicon carbide (SiC) is a promising material for semiconductor device applications designed to operate at high temperature and radiation fields due to its wide band gap, high saturated electron velocity and high thermal conductivity [1,2]. Physical properties of SiC, for example, band gap, electron and hole mobility are different depending on its polytypes [3]. Above all, 4*H*-SiC has an advantage for utilization to high power devices due to its wide bandgap (3.2 eV). It is also attractive that thermal oxide layer can be grown on SiC, which is needed for metal/oxide/semiconductor field effect transistor (MOSFET). However, in spite of many extensive works [4–8], the density of charged interface defects and interface states in ordinarily produced SiO_2/SiC interface still remains in the range of 10^{11} to 10^{12} cm^{-2}, which is about two orders of magnitude higher than those for SiO_2/Si interfaces [9–12]. Because they eventually reduce the channel mobility and hence prevent the fast operation of SiC–MOS devices, the reduction of these centers is an important issue for MOS applications. The origin of the defects at SiO_2/SiC interfaces should be needed.

Positron annihilation spectroscopy (PAS) is a powerful tool to detect open-volume defects in solids [13,14]. This technique is in general extremely sensitive, indicating observable changes at defect density as low as 10^{-15} cm^{-3} [15,16]. Positrons are efficiently trapped by open-volume defects due to their positive charge. If using a slow positron beam, a depth profiling of defects in a subsurface region with typical depth of several microns is possible. This fact indicates that the PAS technique can be used to characterize defects near SiO_2/SiC interface. Indeed, previous positron annihilation studies suggest the existence of open-volume type defects at SiO_2/Si interfaces and their passivation with some specific treatments [17–21].

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Successful positron studies on SiO_2/Si interface owes to the fact that positrons are drifted by applying bias voltage similar to holes. In this study, we investigate the characteristics of the SiO_2/SiC interface in SiC–MOS made by pyrogenic and dry oxidation methods using PAS and capacitance–voltage (C–V) measurements.

2. Experimental

Crystals used in this study (10 mm in squire) were made by cutting from 2 in. CVD-grown n- and p-type 4*H*-SiC epilayers on 8°-off oriented 4*H*-SiC(0 0 0 1) substrates purchased from Cree Research Inc. The net donor concentration of the epilayers was about 5×10^{15} cm^{-3}. The samples were boiled with acetone and sulfuric acid to degrease their surfaces and sacrifice oxidation was performed twice. Two types of MOS samples were fabricated; oxidations were performed by pyrogenic oxidation at 1100 °C for 2 h or by dry oxidation at 1200 °C for 3 h. The oxide thickness was approximately 40 nm. Aluminum (250 Å thick) was deposited on these oxides as gate electrodes (9 mm × 9 mm). To make ohmic contacts, oxides grown on backside substrates were removed and aluminum was evaporated on the exposed surfaces of them.

Fig. 1 shows the schematic arrangement of the positron experimental setup. Positrons generated by a positron source (^{22}Na, 1.11 GBq) are thermalized in a tungsten moderator with a thickness of 6 μm. Slow positrons emitted from the moderator are extracted by a grid electrode (0.2 kV) and transported by a magnetic guiding field (~0.02 T). To suppress backgrounds due to fast positrons and γ-rays coming from positron source directly, this guiding field is bended to an angle of 90°. Positrons with energies from 0.2 to 20 keV were injected into the MOS samples through the Al electrodes. The bias voltage of the gate was changed in the range from −36 to +15 V. There is no damage of the sample by positron irradiation due to the low intensity of positrons (~10^4 e$^+$ s^{-1}). The implanted positrons lose their energy rapidly, diffuse and finally annihilate with electrons emitting mostly two gamma quanta (~511 keV). The energy spectrum of the annihilation γ-ray is Doppler-shifted depending on the momentum of the electron–positron pair before annihilation. As the momentum distribution of electrons in defects is different from that in bulk, defects are detected through measurements of Doppler broadening profiles of the annihilation γ-ray. The Doppler spectra measured by a high resolution Ge detector were quantified by so-called *S*-parameter, which is defined as the normalized peak intensity of the Doppler spectrum. The value of *S*-parameter tends to increase at open-volume type defects because of the narrowing of the Doppler spectrum due to the reduction of core electron annihilation rate which gives rise to a greater Doppler-shift. All the *S*-parameters were normalized to the *S*-parameter of SiC substrate.

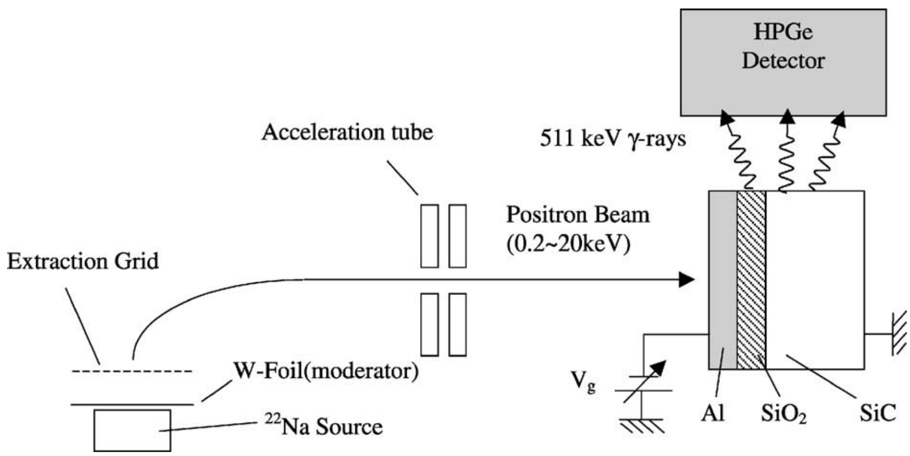

Fig. 1. Schematic drawing of experimental setup.

3. Results and discussion

Positrons feel the electric field in the oxide and the SiC interface region like charged carriers. Positrons and holes have the same charge, however, their motion in a MOS structure will be different. We first describe basic behavior of positrons in MOS physics. In an ideal MOS capacitor, the Fermi level will be equal in three layers without external field and hence no internal electric fields appears. This is called ‘flatband condition’. In a real MOS structure, band bending will occur at the SiO_2/SiC interface due to charges existing at the oxide layer and the interface. This electric field is canceled by an external bias voltage applied to the MOS system. This voltage is the flatband voltage (V_{fb}). In the flatband condition, positrons implanted into the MOS structure will diffuse freely. A MOS structure applying bias voltages ($V_g > V_{fb}$ for n-type and $V_g < V_{fb}$ for p-type) to collect majority carriers to the interface is in ‘accumulation’. In accumulation condition of p-type MOS, positrons implanted at near the interface are influenced by an internal field. In accumulation condition of n-type MOS, positrons implanted at near interface will move towards the substrate similar to holes. MOS system biased suppressing of concentration of majority carriers to the interface is in the ‘depletion’. The external field ($V_g < V_{fb}$ for n-type and $V_g > V_{fb}$ for p-type) is terminated at the ionized dopant atoms in the depleted regions. Positrons implanted at depletion region will feel electric field effectively. Hence, positrons in the n-type MOS are gathered to the SiO_2/SiC interface. In the case of Si–MOS the external field balances with minority carriers for higher fields. The MOS structure is called ‘inversion’. Once the inversion begins, the width of the depletion layer remains constant. However, in case of SiC–MOS structure the depletion layer remains extending without forming inversion layer because of slow response of minority carrier at the room temperature. Therefore positrons implanted at deeper regions will be still influenced by the electric field.

Fig. 2 shows the measured S-parameter as a function of incident positron energy (E) from 0.2 to 20 keV at different gate bias (V_g) for n- and p-MOS samples made by pyrogenic oxidation. At $V_g = 0$ V, S-parameter remains constant in higher incident energy region ($E > 8$ keV). This shows that most positrons are implanted into SiC epitaxial layers and annihilate there. Positrons with lower energy (<2 keV) are implanted into SiO_2 or Al layers. A little reduction of S-parameters at $E = 0.2$ keV indicates the positron annihilation at the surface of the MOS. A high S-parameter at 1 keV regions can be attributed to the annihilation of positrons in the Al layer. Positron annihilation due to SiO_2 layer corresponds to 1 keV $< E <$ 2 keV. Hence the energy regions at 2 keV $< E <$ 8 keV reflect the properties of SiO_2/SiC interface.

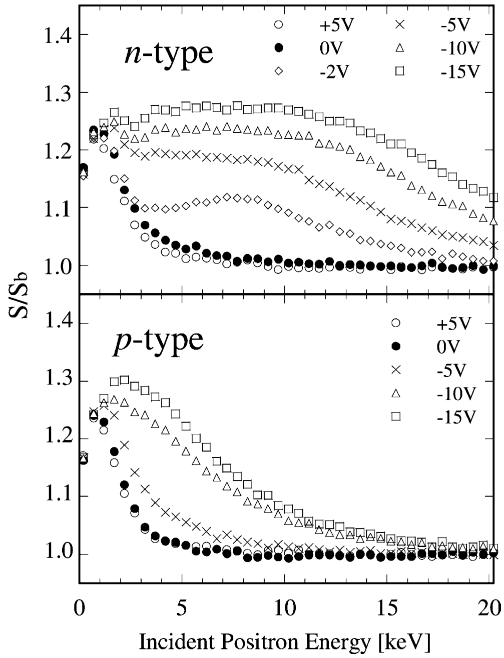

Fig. 2. S-Parameters as a function of incident positron energy at various gate bias (V_g) for n- and p-MOS structures made by pyrogenic oxidation.

Applying the negative gate bias, a substantial change in the shape of the S–E curves is observed in n-MOS. The increase of S-parameter at $E > 2$ keV indicates that positrons drift back towards the SiO_2/SiC interface with gate bias and get trapped by open-volume type defects. The increasing in S-parameters in n-MOS extends higher incident positron energy, i.e. deeper region than in p-MOS. This means that positrons in n-MOS drift more easily toward the interface because of the formation of a depletion layer appears in at SiO_2/SiC interface as expected above. Moving positrons eventually annihilate at some open spaces giving rise the increase in S-parameter. The relatively

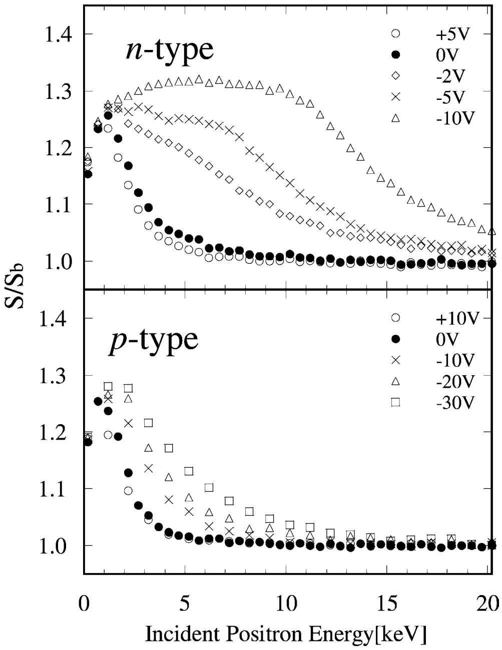

Fig. 3. *S*-Parameters as a function of incident positron energy at various gate bias (V_g) for n- and p-MOS made by dry oxidation.

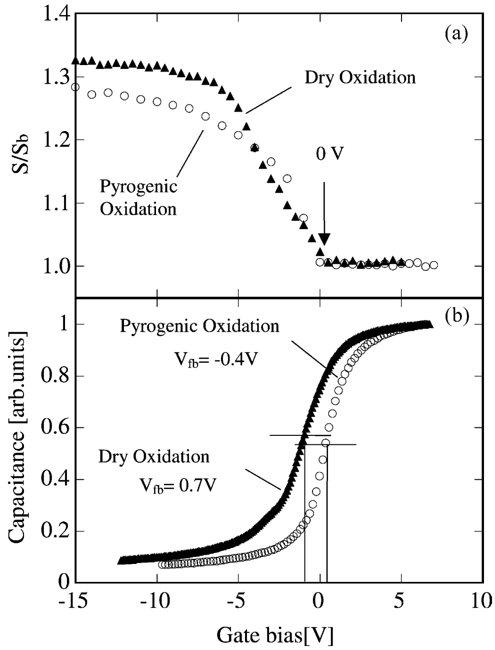

Fig. 4. *S*-Parameters as a function of gate bias voltages at $E = 8$ keV for n-MOSs. Arrows show the threshold voltages for the increases of *S*-parameters.

small increases of *S*-parameter in p-MOS are observed probably because a depletion layer is not formed due to accumulated holes. If $V_g > 0$, no rise of the *S*-parameter is observed. This is because positrons drift toward the SiC substrate by electric field.

Fig. 3 shows positron data on dry oxidation. Distinct differences from the case of pyrogenic oxidation were observed. That is, for n-type MOS, the *S*-parameter is higher than that for pyrogenic oxidation at the same bias voltage. As increasing incident positron energy, the *S*-parameter is reduced more rapidly than in n-type MOS made by pyrogenic oxidation (Fig. 2). This indicates that the electric field in the MOS structure fabricated by dry oxidation does not extend into deeper region due to the narrower depletion layer. Indeed, from the analysis of *C*–*V* characteristics, widths of depletion layers of the n-MOSs at $V_g = -5$ V were determind to be 850 and 570 nm for the pyrogenic and dry oxidations, respectively. The rapid decrease of *S*-parameter in the *S*–*E* curve in the high energy region for the dry oxidation (Fig. 3) can be explained as due to the narrow depletion layer.

To demonstrate the response of *S*-parameter to gate bias voltage more in detail, *S* versus V_g curves were determined at the incident positron energy of 8 keV, where most positrons are implanted into the SiC close to the SiO_2/SiC interface. Fig. 4(a) shows obtained *S*–*V* curves for n-type MOSs with different oxidation. The *S*-parameter rapidly increases from near 0 V in both samples. Fig. 4(b) also shows the results obtained from *C*–*V* measurements for the same MOSs. From these results, the flatband voltages (V_{fb}) are estimated to be approximately 0 V. This closely matches corresponds with the threshold voltages for the increases in *S*-parameters in Fig. 4(a). Fig. 5(a) and (b) show the obtained *S*–*V* curves and *C*–*V* curves for the p-MOSs. For MOS made by pyrogenic oxidation, *S*-parameter starts to increase at $V_g = -3.5$ V. In case of MOS made by dry oxidation, the rapid increase of *S*-parameter is not appeared. However, the rate of the increase changes near −25 V. These seem to change near V_{fb}.

The net number of interface traps per unit area (N_{it}) obtained for n-MOS sample made by the dry oxidation using photo-*CV* technique [22,23] is one order of magnitude higher than that made by the pyrogenic

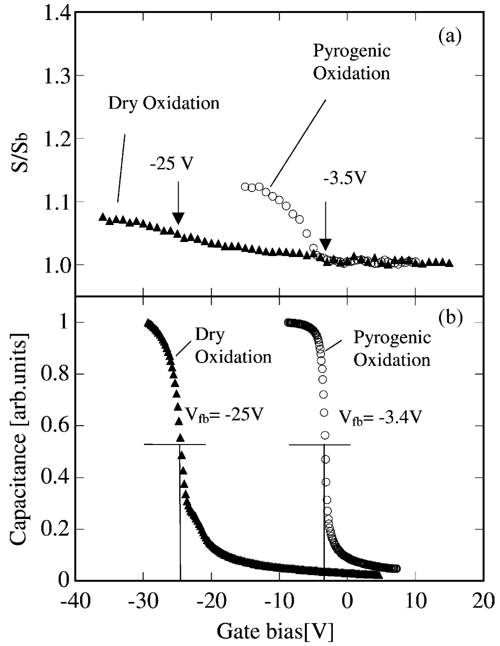

Fig. 5. *S*-Parameters as a function of gate bias voltages at $E = 8$ keV for p-MOSs. Arrows show the threshold voltages for the increases of *S*-parameters.

oxidation. It is interesting to note that *S*-parameter of MOS sample made by dry oxidation is higher than pyrogenic one at $V_g < -3.5$ V as shown in Fig. 4(a), although we hardly find a similar correlation in the case of p-MOS.

Thus, changes of *S*-parameter is affected by oxidation process and conduction type of the substrate. This fact means that positrons drift by following the electric charge which arose in the SiO_2/SiC interface and the positron annihilation properties reflect the condition of the SiO_2/SiC interface. It is necessary to clarify the cause of the increase of the *S*-parameter by applied negative electric field. Clement reported that collected positrons reach gate electrode passing through the interface and oxide film, when negative gate bias is applied to Si–MOS [24–26]. In the case of SiC–MOS, positrons may also pass through the oxide layer. However, it seems to be difficult to consider that all positrons simply pass the SiO_2 layer and annihilate at the gate material. Because there are some incomprehensible phenomena; the characteristic bumps on the *S*–*E* curve, higher *S*-parameter over the value of the aluminum and a correlation between *S*-parameters and N_{it}. It is necessary to clarify such characteristic behavior in detail by the theoretical analysis using the one-dimensional diffusion equation in future. In addition, the quantitative analysis can be possible if the accurate *S*-parameters of defects could be obtained.

4. Summary

We studied defects in SiO_2/SiC interfaces using MOS structures by means of a slow positron beam. By applying negative gate bias, increases of *S*-parameters were observed. This means that positrons implanted into SiC-epilayer drift back to the SiO_2/SiC interfaces. The positron data were compared with results of the *C*–*V* measurements. The flatband voltage and threshold voltage for *S*-parameters are correlated. High interfacial state density corresponds to high *S*-parameter. These facts imply that positrons are trapped at open-volume type defects near the SiO_2/SiC interfaces.

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